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Report #2, Feb 2nd, 2014

**Report on “Dual-ALU CRISC architecture and its compiling technique”**

The article is an analysis and evaluation of Dual-ALU CRISC(a Reduced Instruction Set Computer for the C language) architecture and compiling. CRISC is a high-performance 32-bit RISC processor. Its design base on the following rules: hardware should be kept simple to facilitate a high click rate; there should be a multifunctional-unite support for fine-grained parallel execution; task of instruction scheduling is left to software, but complexity of software should be reduced in some way by architecture design. It has many superiorities because its simultaneous execution architecture on multiple instructions. Depends on the advance of VLSI technology, hardware cost has been decreased. To minimize the disadvantage of increasing the number of pipeline stages obviously increases degree of parallelism, CRISC is separated into I-unit and E-unit which have their own pipelines and different running speed.

The paper focuses on the architectural modelling and the effects of multi-functional units in the CRISC design. Authors use detailed block diagram to illustrate the microarchitecture of the two units of Dual-ALUS CRISC. As to pipeline structure, I-unit has only two stages which are prefetch and preprocessing, while E-unit has three processes which includes read, execution and write back. The authors also analysis the algorithm of its “look-ahead rearrangement code” in the local and global scopes. Besides, they calculate the average cycle time needed of each instruction under reasonable assumption. Compared with normal instruction compaction and 16MHz/30MHz MIPS, they found that penalty of cache misses can be reduced effectively by prefetch scheme, and penalty of a control transfer instruction can be alleviated by compiler effort.

At last, authors get a conclusion that Dual-ALU architecture has been proven a viable option in achieving a high-performance general-purpose CPU with a minimal cost increase. CRISC adopts a multifunctional-unit approach, however, some difficulties induced still need to be avoid carefully. And they will do further study concentrate on code scheduling.

**Reference**

[1] Hong-Chich Chou, Chung-Ping Chung, Shyi-Chyi Cheng, “Dual-ALU CRISC architecture and its compiling technique”, Special issue: Computers Elect. Engng Vol. 17, No. 4, pp. 297-312, 1991, Great Britain, doi: 10.1016/0045-7906(91)90014